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SCULLY SCOTT MURPHY & PRESSER, PC
400 GARDEN CITY PLAZA
SUITE 300
GARDEN CITY, NY 11530

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MAI, ANH D	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/717,279	KOESTER, STEVEN J.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-9,22 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,22 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. The Amendments filed February 23, 2009 is acknowledged. Claims 1, 2 and 7-9 has been amended. Non-elected invention, claims 10-21 have been cancelled. Claims 22 and 23 have been added. Claims 1, 2 and 4-21 are pending. Action on merits of claims 1, 2 and 4-9 follows.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

The specification fails to provide support for the impurity of group IV, i.e., Pb, Sn and C, can form dopant type in the semiconductor material.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1, 2 and 4-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

With respect to claim 1, claim 1 recites: "a first strain layer of semiconductor material doped of a **first dopant type** located on a substrate … a peak concentration of blocking impurity dopant materials selected from the group *consisting of* **In, Pb, Sb and Sn** ...".

Among the four dopant materials listed above, only In and Sb are well known in the art to form a conductivity type in the semiconductor material 110/120.

What is the **dopant type** formed by **Pb or Sn**?

Claims 1, 2 and 4-6, therefore, fail to enable one having ordinary skill in the art how to **form the first type dopant utilizing Pb and Sn impurities**.

With respect to claims 7-9, these claims recite: the semiconductor field-effect transistor device as claimed in ***claim 22***, wherein said blocking impurity **is a neutral-type impurity** (claim 7); **is a group IV impurity** (claim 8); and **dopant comprises C, singly or in combination with said Sn or Pb** (claim 9).

Similar to claim 1 above, claim 22 recites: "a first strain layer of semiconductor material doped of a **first dopant type** located on a substrate; …".

It is well known in the art that the **neutral-type impurity**, group IV impurity and C, Sn and Pb **do not from "dopant type"** in the semiconductor substrate such as semiconductor material 110/120.

Similar to claim 1 above, Claims 7-9 fail to enable one having ordinary skill in the art how to **form the first type dopant utilizing materials selected from group IV impurity**.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 9 is further rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 9 recites the limitation "the semiconductor field-effect transistor device as claimed in ***claim*** 22, wherein said blocking impurity dopant comprises C, singly or in combination with **said Sn or Pb**"" in lines 1-3. There is insufficient antecedent basis for this limitation in the claim.

The blocking impurity of the independent claim 22 is a "dopant type" impurity and **does not include Sn or Pb**.

Claim 9 lacks antecedent basis, thus, claim 9 is indefinite.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 4-9, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xiang (U.S. Patent No. 6,749,527) in view of Applicant Admitted Prior Art (AAPA) and Noda et al. (U.S. Patent No. 6,432,802) all of record.

With respect to claim 1, As best understood by Examiner, Xiang teaches a semiconductor field-effect transistor device substantially as claimed including:

a first strained layer (42) of semiconductor material doped of a first dopant type (halo, not shown) located on a substrate (40);

a source region and a drain region (60) implanted with dopants of a second opposite type located at least within the first strain layer (42);

a gate electrode (54) separated from the strained layer (42) by a dielectric region (56), and positioned between the source and drain regions (60);

substrate (40) having one or more threading dislocations, misfit dislocations or crystal defects that extends continuously from the source region to the drain region (60) at the interface between the first strained layer (42) of semiconductor material and substrate (40), and

blocking impurity dopant (halo) materials located substantially at the interface, wherein the blocking impurity dopant (halo) materials partially or fully occupies each of the one or more threading dislocations, misfit dislocation or crystal defects at the interface and substantially inhibit diffusion of the implanted source and drain dopants (60) from diffusing along the threading dislocations, misfit dislocations or crystal defect along the interface. (See Fig. 3i).

Regarding the limitation: *substrate having one or more threading dislocations, misfit dislocations or crystal defects that extends continuously from the source region to the drain*

region at the interface between the first strained layer of semiconductor material and the substrate, according to the AAPA, the *threading dislocations, misfit dislocations or crystal defects* are inherently occurred when the strained layer is grown on the relaxed layer due to the lattice mismatch between two layers. (See [0004]).

The blocking impurity dopant material of Xiang comprises halo regions (first dopant type) implanted using low energy at a small angle, to suppress short channel punchthrough. Moreover, Xiang does use a neutral species, carbon, for the same intended purpose.

Thus, Xiang is shown to teach all the features of the claim with the exception of explicitly disclosing the peak concentration is located substantially at the interface; and utilizing **In**, Pb, **Sb** and Sn for the blocking impurity dopant materials.

However, Noda teaches that it is well known in the art to form the halo region to block the encroachment of the source and drain dopants into the channel region utilizing indium (**In**) and antimony (**Sb**).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the halo blocking region of Xiang utilizing **In** or **Sb** blocking impurity as taught by Noda to prevent diffusion of the source/drain dopants into the channel region.

Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of it suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416., 125 USPQ 416.

Moreover, the first dopant type, halo region, of Noda is formed by implanting the first dopant type at a low energy approximate that of the instant invention, 30 keV, thus, the peak concentration of the blocking impurity, i.e., first dopant type, is obviously approximate the interface as claimed.

With respect to claim 2, the first strained layer (42) of semiconductor material of Xiang comprises material selected from the group comprising Si.

With respect to claim 4, the semiconductor substrate (40) of Xiang includes a SiGe relaxed substrate.

With respect to claim 5 and 6, the device of Xiang includes NMOS and PMOS; and the halo regions, blocking impurity dopant, or first dopant type, is formed of dopant that is opposite the conductivity type of the source and drain.

It is well known in the art that P, As or Sb singly or in combination are dopants for forming source and drain regions in an NMOS; and B or In singly or in combination are dopants for forming source and drain regions in a PMOS.

Therefore, in view of Noda, blocking impurity of In or Sb are well known to be used for halo regions in NMOS and PMOS, respectively, to prevent diffusion of the source/drain dopants into the channel region.

With respect to claim 22, Xiang teaches a semiconductor field-effect transistor device substantially as claimed including:

a first strained layer (42) of semiconductor material doped of a first dopant type (halo, not shown) located on a substrate (40);

a source region and a drain region (60) implanted with dopants of a second opposite type located at least within the first strain layer (42);

a gate electrode (54) separated from the strained layer (42) by a dielectric region (56), and positioned between the source and drain regions (60);

substrate (40) having one or more threading dislocations, misfit dislocations or crystal defects that extends continuously from the source region to the drain region (60) at the interface between the first strained layer (42) of semiconductor material and substrate (40), and

blocking impurity dopant (halo) materials located substantially at the interface, wherein the blocking impurity dopant (halo) materials partially or fully occupies each of the one or more threading dislocations, misfit dislocation or crystal defects at the interface and substantially inhibit diffusion of the implanted source and drain dopants (60) from diffusing along the threading dislocations, misfit dislocations or crystal defect along the interface. (See Fig. 3i).

Regarding the limitation: *substrate having one or more threading dislocations, misfit dislocations or crystal defects that extends continuously from the source region to the drain region at the interface between the first strained layer of semiconductor material and the substrate,* according to the AAPA, the *threading dislocations, misfit dislocations or crystal defects* are inherently occurred when the strained layer is grown on the relaxed layer due to the lattice mismatch between two layers. (See [0004]).

The blocking impurity dopant material of Xiang comprises halo regions (first dopant type) implanted using low energy at a small angle, to suppress short channel punchthrough.

Thus, Xiang is shown to teach all the features of the claim with the exception of explicitly disclosing the peak concentration is located substantially at the interface.

However, Noda teaches a semiconductor field-effect transistor device including forming the halo regions by implanting the first dopant type at a low energy approximate that of the instant invention, 15 keV, thus, the peak concentration of the blocking impurity, i.e., first dopant type, is obviously approximate the interface as claimed.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the halo blocking region of Xiang by implanting the first dopant type at low energy as taught by Noda to prevent diffusion of the source/drain dopants into the channel region, thus suppressing punchthrough.

With respect to claim 7, the blocking impurity of Xiang also includes a neutral-type impurity.

With respect to claim 8, the blocking impurity of Xiang also includes a group IV impurity.

With respect to claim 9, the blocking impurity of Xiang also includes C.

With respect to claim 23, Xiang teaches a semiconductor field-effect transistor device substantially as claimed including:

a first strained layer (42) of semiconductor material doped of a first dopant type (halo, not shown) located on a substrate (40);

a source region and a drain region (60) implanted with dopants of a second opposite type located at least within the first strain layer (42);

a gate electrode (54) separated from the strained layer (42) by a dielectric region (56), and positioned between the source and drain regions (60);

substrate (40) having one or more threading dislocations, misfit dislocations or crystal defects that extends continuously from the source region to the drain region (60) at the interface between the first strained layer (42) of semiconductor material and substrate (40), and

blocking impurity dopant (halo) materials located substantially at the interface, wherein the blocking impurity dopant (halo) materials partially or fully occupies each of the one or more threading dislocations, misfit dislocation or crystal defects at the interface and substantially inhibit diffusion of the implanted source and drain dopants (60) from diffusing along the threading dislocations, misfit dislocations or crystal defect along the interface. (See Fig. 3i).

Regarding the limitation: *substrate having one or more threading dislocations, misfit dislocations or crystal defects that extends continuously from the source region to the drain region at the interface between the first strained layer of semiconductor material and the substrate,* according to the AAPA, the *threading dislocations, misfit dislocations or crystal defects* are inherently occurred when the strained layer is grown on the relaxed layer due to the lattice mismatch between two layers. (See [0004]).

The blocking impurity dopant material of Xiang comprises halo regions (first dopant type) implanted using low energy at a small angle, to suppress punchthrough.

Thus, Xiang is shown to teach all the features of the claim with the exception of explicitly disclosing the peak concentration of the blocking impurity dopant material, first dopant type, is located substantially at the interface; and having a concentration between 10^{17} cm^{-3} to 10^{19} cm^{-3}.

However, Noda teaches a semiconductor field-effect transistor device including forming the halo regions by implanting the first dopant type at a low energy approximate that of the instant invention, 15 keV, at a dose of 10^{14} cm^{-2} to 10^{16} cm^{-2}, thus, the peak concentration of the blocking impurity, i.e., first dopant type, is obviously approximate the interface and the concentration, between 10^{17} cm^{-3} to 10^{19} cm^{-3}, as claimed.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the halo blocking region of Xiang by implanting the first dopant type at low energy and dose as taught by Noda to prevent diffusion of the source/drain dopants into the channel region, thus suppressing punchthrough.

Response to Arguments

7. Applicant's arguments with respect to amended and new claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Anh D. Mai/
Primary Examiner, Art Unit 2814